REMARKS

The priority information in the specification has been updated to indicate that parent U.S. patent application 10/054,653 is now allowed.

Allowed independent Claims 95 and 107 each require that each gate electrode portion of the recited varactor be (I) of different conductivity type than each other gate electrode portion or/and (II) of different average net dopant concentration than each other gate electrode portion. Claims 95 and 107 are, for convenience, repeated below with conditions I and II bolded for emphasis:

95. A method comprising:

selecting a varactor that comprises (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a gate dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the gate dielectric layer at least where the gate dielectric layer contacts material of the body region, the plate and body regions being of opposite conductivity types, meeting each other to form a p-n junction, and extending to a primary surface of the semiconductor body, the plate region occupying a lateral plate area along the primary surface, the varactor having a minimum capacitance dependent on the plate area, a field insulating region extending into the semiconductor body along the primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions, the semiconductor island occupying a lateral island area along the primary surface, the varactor having a maximum capacitance dependent on the island area, the gate electrode comprising multiple gate electrode portions which are of doped semiconductor material and which at least partially overlie the body region, **each gate electrode portion being of different conductivity type or/and different average net dopant concentration than each other gate electrode portion**; and

adjusting the plate and island areas to control the minimum and maximum capacitances of the varactor.

107. A method comprising:

selecting a varactor that comprises (a) a plate region and a body region of a semiconductor body, (b) a plate electrode and a body electrode respectively connected to the plate and body regions, (c) a gate dielectric layer situated over the semiconductor body and contacting the body region, and (d) a gate electrode situated over the gate dielectric layer at least where the gate dielectric layer contacts material of the body region, the plate and body regions being of opposite conductivity types, meeting each other to form a p-n junction, and extending to a primary surface of the semiconductor body, the plate region occupying a lateral plate area along the primary surface, the

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varactor having a minimum capacitance dependent on the plate area, the body region occupying a lateral body area along the primary surface, the varactor having a maximum capacitance dependent on the body area in combination with the plate area, the gate electrode comprising multiple gate electrode portions which are of doped semiconductor material and which at least partially overlie the body region, **each gate electrode portion being of different conductivity type or/and different average net dopant concentration than each other gate electrode portion**; and

adjusting the plate and body areas to control the minimum and maximum capacitances of the varactor.

Varactor condition I that each gate electrode portion be of different conductivity type than each other gate electrode portion is verbally described in paragraphs 186 - 193 of the specification and illustrated in application Fig. 14. The gate electrode portions for condition I are implemented with n++ polycrystalline silicon ("polysilicon") lower gate electrode portion 112LA and p++ polysilicon lower gate electrode portion 112LB that meet to form pn junction 190 as depicted in Fig. 14.

Varactor structures which meet condition II that each gate electrode portion be of different average net dopant concentration than each other gate electrode portion are verbally described in paragraphs 194 and 195 of the specification as variations of the varactor of Fig. 14. However, varactor structures meeting condition II are not illustrated in the drawings as originally filed. In light of the requirement of 37 CFR 1.83(a) that the drawings show every (structural) feature of the invention specified in the claims, Figs. 14.1 and 14.2 are being added to the application's drawings via the accompanying Amendment to Drawings under 37 CFR 1.312 in order to illustrate condition II.

New Fig. 14.1 is a variation of Fig. 14 in which lower gate electrode portion 112LB is changed from p++ polysilicon to n++ polysilicon at a lower average net dopant concentration than the n++ polysilicon of lower gate electrode portion 112LA in accordance with specification paragraph 194. New Fig. 14.2 is a complementary variation of Fig. 14 in which lower gate electrode portion 112LA is changed from n++ polysilicon to p++ polysilicon at a lower average net dopant concentration than the p++ polysilicon of lower gate electrode portion 112LB likewise in accordance with specification paragraph 194. To emphasize that gate electrode portions 112LA and 112LB are of different polysilicon dopant concentrations in Figs. 14.1 and 14.2, portions 112LA and 112LB in each Fig. 14.1 or 14.2 are also

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respectively provided with the labels "N_{POLYA}" and "N_{POLYB}" representing the respective average net polysilicon dopant concentrations of portions 112LA and 112LB.

Polysilicon gate electrode portions 112LA and 112LB are of the same conductivity type in Figs. 14.1 and 14.2. That is, portions 112LA and 112LB are both n type in Fig. 14.1 and both p type in Fig. 14.2. Consequently, pn junction 190 of the varactor of Fig. 14 is not present in the varactor of Fig. 14.1 or 14.2.

The specification has been revised to accommodate Figs. 14.1 and 14.2 without introducing any new matter into the disclosure. In particular, paragraph 51 of the Brief-Description-of-the-Drawings section of the specification has been revised to specify that Figs. 14.1 and 14.2 are now part of the application.

Also, a pair of sentences have been inserted into paragraph 194 to respectively deal with Figs. 14.1 and 14.2. Using the reference notation "N_{POLYA}" and "N_{POLYB}" employed in Fig. 14.1, paragraph 194 now recites that "Such a variation of the varactor of Fig. 14 is depicted in Fig. 14.1 where net polysilicon dopant concentration N_{POLYA} of n++ electrode portion 112LA exceeds net polysilicon dopant concentration N_{POLYB} of n++ electrode portion 112LB". This conforms with the earlier original statement, as corrected in the 9 May 2005 Preliminary Amendment, that "If electrode portions 112LA and 112LB are both n-type and thus of opposite conductivity type to body region 100, electrode portion 112LA is doped more heavily n-type than is electrode portion 112LB".

Similarly using the reference notation "N_{POLYA}" and "N_{POLYB}" employed in Fig. 14.2, paragraph 194 now further recites that "Fig. 14.2 illustrates such a further variation of the varactor of Fig. 14 for which polysilicon dopant concentration N_{POLYA} of p++ electrode portion 112LA is less than polysilicon dopant concentration N_{POLYB} of p++ electrode portion 112LB". This insertion conforms with the earlier original statements, as corrected in the 9 May 2005 Preliminary Amendment, that "The reverse dopant-concentration relationship arises if electrode portions 112LA and 112LB are both p-type and thus of the same conductivity type as body region 100" and "Per Eq. 33, electrode portion 112LA is doped more lightly p-type than is electrode portion 112LB".

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The last sentence of paragraph 194, now split into two paragraphs, originally stated that "Since p-n junction 190 is absent in this variation, upper metallic gate electrode layer 112U can be deleted". In order to better accommodate the addition of Figs. 14.1 and 14.2,

the last sentence of paragraph 194 has been revised to state that "Since p-n junction 190 is absent in the variations of Figs. 14.1 and 14.2, upper metallic gate electrode layer 112U can be deleted in such variations".

As the preceding comments indicate, the material illustrated in newly added Figs. 14.1 and 14.2 is disclosed in the application as filed. Aside from identifying Figs. 14.1 and 14.2, the specification revisions made to accommodate the addition of Figs. 14.1 and 14.2 are supported in the original specification. Accordingly, the addition of Figs. 14.1 and 14.2 and the associated revisions to the specification do not add new matter to the disclosure*.

Entry of the present amendment and the accompanying Amendment to Drawings will not entail materially added work on the Examiner's part. No more than a cursory review of the record will be needed. Accordingly, this amendment and the Amendment to Drawings should be entered.

Please telephone Applicant's Attorney at 650-964-9767 if there are any questions.

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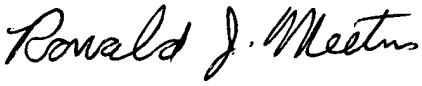
Respectfully submitted,



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* Amendments under 37 CFR 1.312 have been submitted to revise the specification and drawings of parent U.S. patent application 10/054,653 in the way described above in light of a 37 CFR 1.83(a) objection made to the drawings of the parent application.